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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/067,819	02/08/2002	Takayuki Matsubara	60188-150	9583

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	4

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/067,819	MATSUBARA ET AL.	
	Examiner	Art Unit	
	James C Kerveros	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Andrews (US 5459737).

Regarding independent Claim 1, Andrews discloses a built-in current monitor (BIC) and method for monitoring and testing the quiescent current (IDDQ) of an integrated circuit (IC) device, the IC device comprising:

At least two logic circuits (20, FIG. 7) including a first logic circuit and a second logic circuit (CMOS module 1 and 2) respectively each having the same function,

A direction circuit (BICSC TDR 7) bit register provided with a parallel port output coupled respectively to the gates of the bypass transistors (N1, N2) for controlling the conducting states of the transistors associated with logic circuit CMOS module 1 and 2, respectively, according to the BIC monitor bypass code BICBC.

The direction circuit (BICSC TDR 7) directs the operation of (CMOS module 1 and 2) through the externally supplied select signal, test mode select (TMS), which is provided to the TAP controller for controlling the normal or test mode of operation. During the normal operation of the IC device in response to a first BICBC, the bypass

transistor provides a low impedance bypass path around the BIC current monitor. During the test mode in response to a second BICBC, the bypass transistor presents a high impedance bypass path for monitoring quiescent current IDDQ at the BIC monitor.

Regarding Claim 3, Andrews discloses first and second logic circuits (CMOS module 1 and 2), which perform a logic operation during the normal operation of the IC device in response to a BICBC, where the bypass transistor provides a low impedance bypass path around the BIC current monitor.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andrews (US 5459737).

Regarding independent Claim 4, Andrews substantially discloses a method including simultaneously operating the first and second logic circuits (CMOS module 1 and 2) through the BIC monitor circuit for high impedance during the test mode, transferring the outputs of the (BIC 1 and 2) current monitor to a signal line such as fault capture TAP data register BICFCP TDR6, measuring the supply current flowing through

the shunt circuit coupled in parallel with the BIC monitor (FIG. 1) and determining whether the (CMOS module 1 and 2) are defective or non defective using a voltage comparator VCOMP based on the measured supply current.

Regarding Claim 2, Andrews substantially discloses a first output circuit (10, BIC 1) for receiving an output from the first logic circuit (CMOS module 1) and a second output circuit (10, BIC 2) for receiving an output from the second logic circuit (CMOS module 2).

A signal line, such as BIC fault capture TAP data register BICFCP TDR6 having parallel port inputs and coupled to the respective BIC outputs for receiving and storing the fault signals (F), and outputting the fault signals through a serial port output by serially shifting out the fault signals F at the TDO pin for analysis in compliance with IEEE Standard 1149.1.

The first and second output circuits (10, BIC 1 and 2) enter an enable state during the test mode in response to an externally supplied testing mode signal (TMS) in response to a BICBC, where the bypass transistors (N1, N2) presents a high impedance bypass path for monitoring quiescent current IDDQ at the BIC monitor.

Regarding Claims 2 and 4, Andrews does not explicitly measure the supply current flowing through a signal line, which receives both the outputs of the first and second output circuits. However, Andrews discloses BIC 1 and 2 for measuring the quiescent IDDQ current corresponding to (CMOS module 1 and 2) respectively, during the test mode and in turn combining the measuring results in the TDR6 register for receiving and storing the fault signals F, which incorporates a serial port output for

serially shifting out the fault signals F for analysis at the TDO pin. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a parallel to serial shift register, as taught by Andrews, to combine the individual parallel current measurements into one signal line by serially shifting out the fault signals F for analysis at the TDO having IEEE Standard 1149.1 compliance for interfacing with a BITE circuitry via the TAP controller. Since the built-in current monitor (BIC) fabricated on the chip reduces parasitic capacitance, inductance, and consequent delays for static current testing, which has an advantage over the use of external automatic test equipment (ATE) which introduces substantial parasitic capacitance, inductive reactance and increasing the time to quiescent conditions following switching events and slowing the rate of IDDQ testing, (col. 2, lines 5-20).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 3 June 2004
Office Action: Non-Final Rejection

By: _____

James C Kerveros
Examiner
Art Unit 2133

Gary J. Lamarre
for

Albert DeCady
Primary Examiner